EMI&ESD Design for USB2.0

USB (Universal Serial Bus) port providing bidirectional and real-time date transfer, has many merits, such as Plug and Play, hot swap, low cost, etc. At the present day USB has been your preferred and instant connection to computers and peripherals. USB 2.0 has a raw data rate at 480Mbps, and it is rated 40 times faster than its predecessor interface, USB 1.1 which tops at 12Mbps and USB 1.0 which tops at 1.5Mbps. USB 1.1 and USB 1.0 are now obsolete, but both of its speeds are being adopted into USB 2.0, which is called backward compatibility. USB 2.0 makes data exchanging faster and more usable for digital photography or the limitless creative possibilities of digital imaging. Another USB port worthy of note is USB OTG, the USB promoter group, which can realize devices to communicate to each other when moving away from a PC-centric world. For example, digital cameras can directly connect to printers to print photos, and PDAs can directly content to other PDAs to send images.

To maintain high speed transfer of USB group, It is important and critical for USB design to improve signal quality, minimize infection of EMI and ESD. This document will study and discuss based on two aspects of circuit design and PCB layout.

EMI Design

When high speed differential mode signals transmit by USB 2.0 port, signal wobble in ground lines and power lines will cause radiated noise increasing sharply. To avoid crosstalk and assure signal integrity, it is a necessary countermeasure of EMI design to。

As **Fig.1** shows, ferrite beads **PZ2012U121-2R0**, with impedance of 120ohm and rated current of 2A are connected in series to VDD line and ground line respectively, and common mode choke coil **SDCL2012-2-900** with impedance of 120ohm is connected to differential signal lines. The common mode choke coil is a winding core wrapped by two copper wires in the same direction. Magnetic flux caused by common mode current accumulates and high impedance is produced. On the opposite magnetic flux caused by differential mode current cancels each other and no impedance or low impedance is produced.

As for **SDCW2012-2-900,** differential mode impedance is only 4.6ohm at 100MHz and the product of common mode choke won't distort signal which attenuation characteristic curve also shows as **Fig 2**. The common mode choke coil could suppress signal distinguished by current.

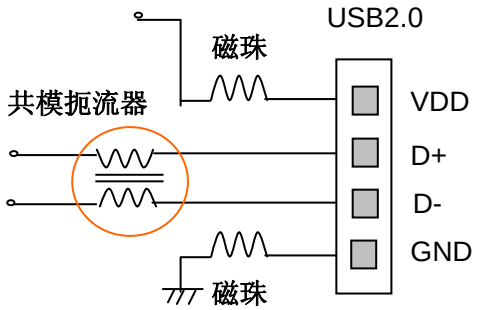

Fig.1

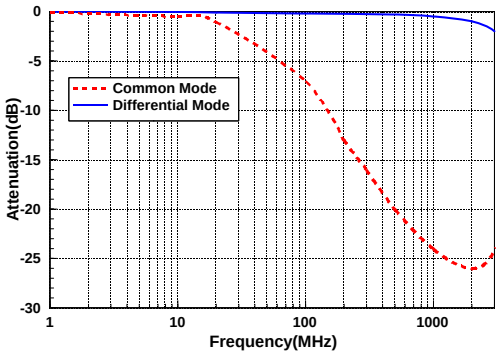

Fig.2

ESD Design

The damage of ESD exists everywhere, and moreover every time the device is connected or disconnected, the circuit receives a voltage transient. ESD is one such transient which would damage to read error, system down, burnout of PCB and so on. USB 2.0 needs circuit protection urgently to work smoothly and reliable.

Fig.3 shows chip varistors **SDV1005A5R5C101NPT** with DC working voltage of 5.5V and capacitance of 100pF are connected in parallel to VDD line and ground line respectively. As signal lines achieve data rate of 480Mbps, the paralleled capacitance value is needed to be less than 4pF because of signal integrity. The waveform would deteriorate and even digital bit errors occur due to big capacitance. Therefore chip varistors **SDV1005H180C4R0GPT** with DC working voltage of 18V and maximum capacitance of 4pF are connected in parallel to data lines. **Fig. 4** shows chip varistor with capacitance of 4pF works little on signal waveform.

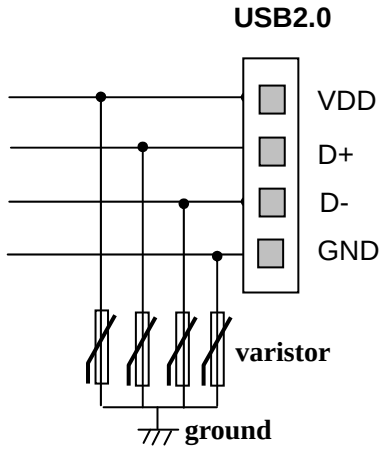

Fig.3

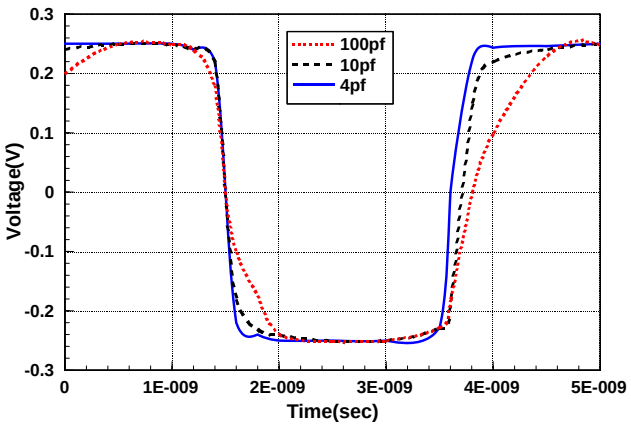

Fig.4

PCB Layout Design

The design guidelines below need to be considered when making PCB layout,

1. The lengths of two conduct traces for differential signal should be compatible, otherwise time sequence would offset and additional EMI would occur resulting in poor signal quality.
2. The space between two conduct traces for differential signal should keep less than 10mm, and the space with other lines should increase much more.
3. The two conduct traces for differential signal should be laid on the same layer. The difference between impedance or through holes which will occur when the two lines was laid on different layers will induce common mode noise to damage signal quality.
4. The coupling between differential signal lines can influence characteristic impedance of signal lines. Terminal resistance must be applied to realize maximum matching for transmission lines.
5. To minish through holes or other factors causing line discontinuity to the maximum extent.
6. To substitute arc lines or 45° fold lines for conduct lines of 90° to avoid impedance discontinuity.
7. To place chip varistor close to I/O port and the ground which chip varistor connect to is shielded