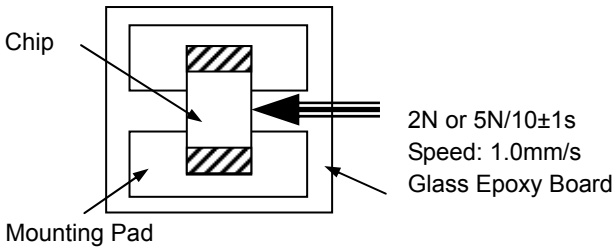
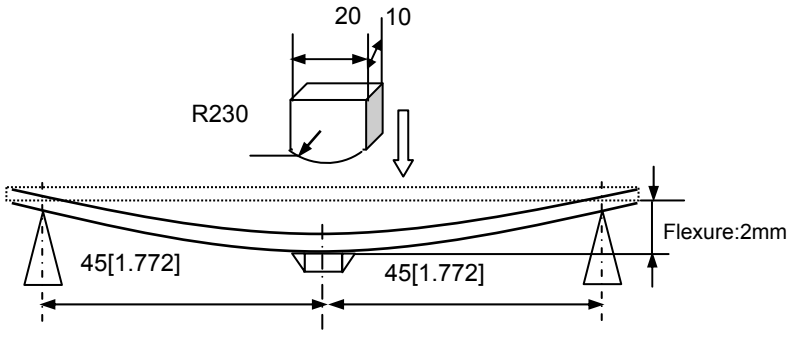
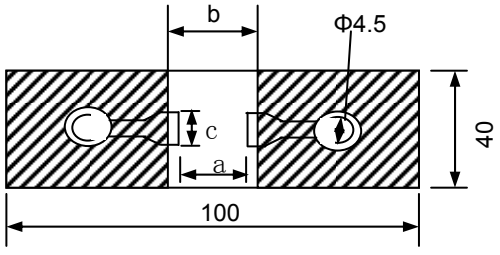
RELIABILITY AND TEST CONDITIONS

Ultra low capacitance Multilayer Chip Varistor (SDV≤2pF Series)

<table>
<tr><th>Items</th><th>Requirements</th><th>Test Methods and Remarks</th></tr>
<tr><td>1. Operating Temperature Range</td><td colspan="2">-55℃ to +125℃</td></tr>
<tr><td>2. Storage Temperature Range</td><td colspan="2">-55℃ to +125℃</td></tr>
<tr><td>3. Terminal Strength</td><td>No removal or split of the termination or other defects shall occur.</td><td>① Solder the chip to the testing jig (glass epoxy board shown as the following figure.) using eutectic solder. Then apply a force in the direction of the arrow.
② 2N force for SDV0603 series.
5N force for 1005 and 1608 series.
③ Keep time: 10±1s
 
</td></tr>
<tr><td rowspan="2">4. Resistance to Flexure</td><td>No visible mechanical damage.</td><td>① Solder the chip to the test jig (glass epoxy board) using a eutectic solder. Then apply a force in the direction shown as the following figure.
② Flexure: 2mm
③ Pressurizing speed: 0.5mm/sec
④ Keep time: 30 sec</td></tr>
<tr><td colspan="2"> 

Unit: mm [inch]
<table>
<tr><th>Type</th><th>a</th><th>b</th><th>c</th></tr>
<tr><td>0603[0201]</td><td>0.25</td><td>0.8</td><td>0.3</td></tr>
<tr><td>1005[0402]</td><td>0.4</td><td>1.5</td><td>0.5</td></tr>
<tr><td>1608[0603]</td><td>1.0</td><td>3.0</td><td>1.2</td></tr>
</table>

</td></tr>
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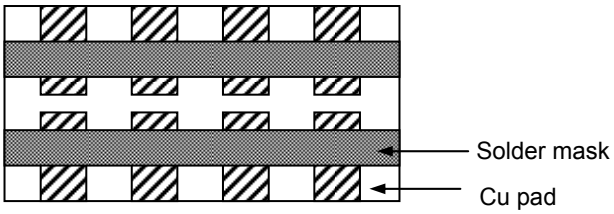
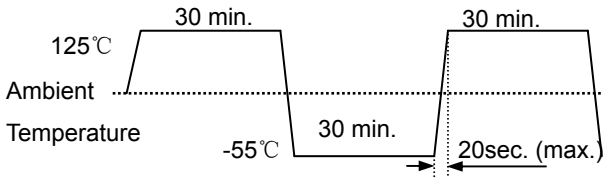
RELIABILITY AND TEST CONDITIONS

Ultra low capacitance Multilayer Chip Varistor (SDV (Cp≤2pF) Series)

Items	Requirements	Test Methods and Remarks
5. Vibration	No visible mechanical damage.	① Solder the chip to the testing jig (glass epoxy board shown as the following figure) using eutectic solder. ② The chip shall be subjected to a simple harmonic motion having total amplitude of 1.5 mm, the frequency being varied uniformly between the approximate limits of 10 and 55 Hz. ③ The frequency range from 10 to 55 Hz and return to 10 Hz shall be traversed in approximately 1 minute. This motion shall be applied for a period of 2 hours in each 3 mutually perpendicular directions (total of 6 hours).  Glass Epoxy Board
6. Solderability	① No visible mechanical damage. ② Wetting shall be exceeded 90% coverage.	① Solder temperature: 240±2℃ ② Duration: 3 sec ③ Solder: Sn/3.0Ag/0.5Cu ④ Flux: 25% Resin and 75% ethanol in weight
7. Resistance to Soldering Heat	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Solder temperature: 260±3℃ ② Duration: 5 sec ③ Solder: Sn/3.0Ag/0.5Cu ④ Flux: 25% Resin and 75% ethanol in weight. ⑤ The chip shall be stabilized at normal condition for 1~2 hours before measuring.
8. Thermal Shock	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature and time: -55℃for 30±3 min→125℃ for 30±3min ② Transforming interval: Max. 20 sec ③ Tested cycle: 100 cycles ④ The chip shall be stabilized at normal condition for 1~2 hours before measuring. 
9. Resistance to Low Temperature	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: -55±2℃ ② Duration: 1000^{+24} hours ③ The chip shall be stabilized at normal condition for 1~2 hours before measuring.
10. Resistance to High Temperature	① No visible mechanical damage. ② Varistor voltage change: within ±10%.	① Temperature: 125±2℃. ② Duration: 1000^{+24} hours. ③ The chip shall be stabilized at normal condition for 1~2 hours before measuring.

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RELIABILITY AND TEST CONDITIONS

Ultra low capacitance Multilayer Chip Varistor (SDV ($C_p \leqslant 2pF$) Series)

Items	Requirements	Test Methods and Remarks
11. Damp Heat (Steady States)	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: 60±2℃ ② Humidity: 90% to 95% RH ③ Duration: 1000^{+24} hours ④ The chip shall be stabilized at normal condition for 1~2 hours before measuring.
12. Loading Under Damp Heat	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: 60±2℃ ② Humidity: 90% to 95% RH ③ Duration: 1000^{+24} hours ④ Applied voltage: DC working voltage ⑤ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
13. Loading at High Temperature (Life Test)	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: 125±2℃ ② Duration: 1000^{+24} hours ③ Applied voltage: DC working voltage ④ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.

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RELIABILITY AND TEST CONDITIONS

Multilayer Chip Varistor (SDV (Cp≥3pF) Series)

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<tr><th>Items</th><th>Requirements</th><th>Test Methods and Remarks</th></tr>
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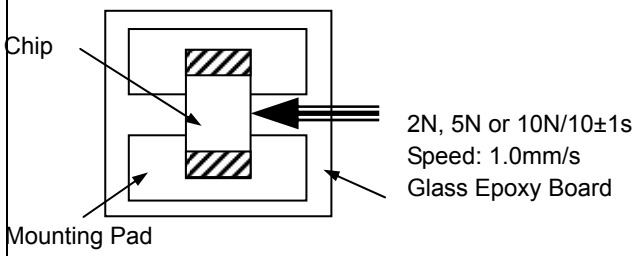
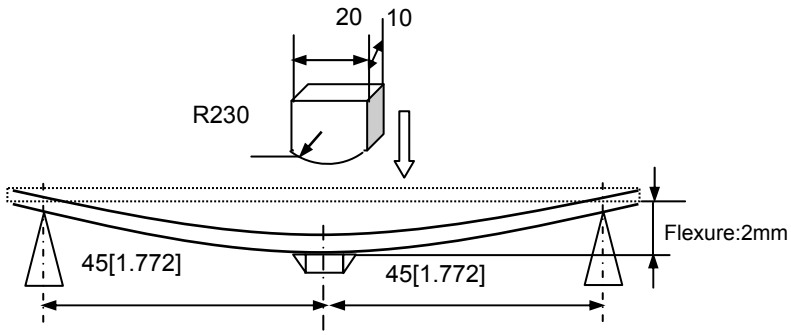
<tr><td>2. Storage Temperature Range</td><td colspan="2">-55℃ to +125℃</td></tr>
<tr><td>3. Terminal Strength</td><td>No removal or split of the termination or other defects shall occur.</td><td>① Solder the chip to the testing jig (glass epoxy board shown as the following figure.) using eutectic solder. Then apply a force in the direction of the arrow.
② 2N force for SDV0603 series.
③ 5N force for 1005 and 1608 series.
④ 10N force for 2012 series.
⑤ Keep time: 10±1s
 
</td></tr>
<tr><td rowspan="2">4. Resistance to Flexure</td><td>No visible mechanical damage.</td><td>① Solder the chip to the test jig (glass epoxy board) using a eutectic solder. Then apply a force in the direction shown as the following figure.
② Flexure: 2mm
③ Pressurizing speed: 0.5mm/sec
④ Keep time: ≥30 sec</td></tr>
<tr><td colspan="2"> 

Unit: mm [inch]
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<tr><td>1608[0603]</td><td>1.0</td><td>3.0</td><td>1.2</td></tr>
<tr><td>2012[0805]</td><td>1.2</td><td>4.0</td><td>1.65</td></tr>
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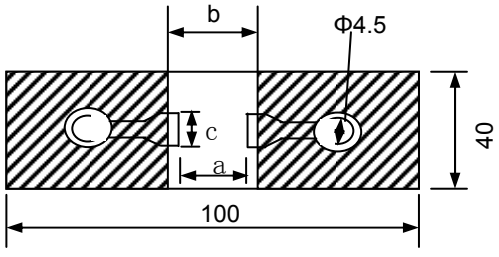
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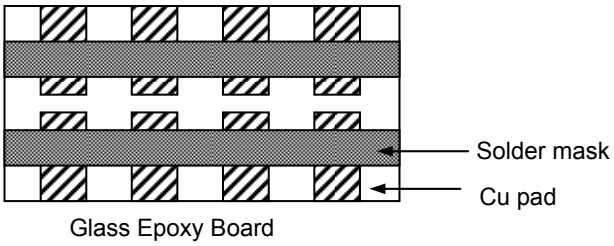
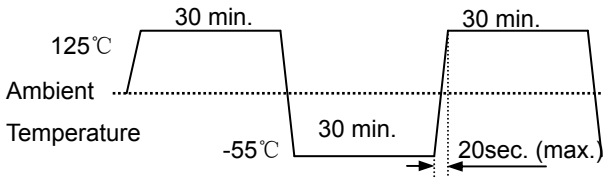
RELIABILITY AND TEST CONDITIONS

Multilayer Chip Varistor (SDV (Cp≥3pF) Series)

Items	Requirements	Test Methods and Remarks
5. Vibration	No visible mechanical damage.	① Solder the chip to the testing jig (glass epoxy board shown as the following figure) using eutectic solder. ② The chip shall be subjected to a simple harmonic motion having total amplitude of 1.5 mm, the frequency being varied uniformly between the approximate limits of 10 and 55 Hz. ③ The frequency range from 10 to 55 Hz and return to 10 Hz shall be traversed in approximately 1 minute. This motion shall be applied for a period of 2 hours in each 3 mutually perpendicular directions (total of 6 hours). 
6. Solderability	① No visible mechanical damage. ② Wetting shall be exceeded 90% coverage.	① Solder temperature: 240±2℃ ② Duration: 3 sec ③ Solder: Sn/3.0Ag/0.5Cu ④ Flux: 25% Resin and 75% ethanol in weight
7. Resistance to Soldering Heat	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Solder temperature: 260±3℃ ② Duration: 5 sec ③ Solder: Sn/3.0Ag/0.5Cu ④ Flux: 25% Resin and 75% ethanol in weight. ⑤ The chip shall be stabilized at normal condition for 1~2 hours before measuring.
8. Thermal Shock	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature and time: -55℃for 30±3 min→125℃ for 30±3min ② Transforming interval: Max. 20 sec ③ Tested cycle: 100 cycles ④ The chip shall be stabilized at normal condition for 1~2 hours before measuring. 
9. Resistance to Low Temperature	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: -55±2℃ ② Duration: 1000^{+24} hours ③ The chip shall be stabilized at normal condition for 1~2 hours before measuring.
10. Resistance to High Temperature	③ No visible mechanical damage. ④ Varistor voltage change: within ±10%.	④ Temperature: 125±2℃. ⑤ Duration: 1000^{+24} hours. ⑥ The chip shall be stabilized at normal condition for 1~2 hours before measuring.

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RELIABILITY AND TEST CONDITIONS

Multilayer Chip Varistor (SDV (Cp≥3pF) Series)

Items	Requirements	Test Methods and Remarks
11. Damp Heat (Steady States)	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: 60±2℃ ② Humidity: 90% to 95% RH ③ Duration: 1000^{+24} hours ④ The chip shall be stabilized at normal condition for 1~2 hours before measuring.
12. Loading Under Damp Heat	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: 60±2℃ ② Humidity: 90% to 95% RH ③ Duration: 1000^{+24} hours ④ Applied voltage: DC working voltage ⑤ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
13. Loading at High Temperature (Life Test)	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: 125±2℃ ② Duration: 1000^{+24} hours ③ Applied voltage: DC working voltage ④ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
14. Maximum Surge Current	① No visible mechanical damage. ② Varistor voltage change: Within ±10%. IEC61000-4-5 standard 1.2/50us-8/20us voltage-current combination pulse	① Temperature: 25±5℃ ② Humidity: 30% to 65% RH ③ Number of hit: each 1 time of +/- polarity. ④ Pulse waveform: 8/20 us ⑤ Applied current: maximum surge current (I_P) ⑥ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
15. Maximum Surge Energy	① No visible mechanical damage. ② Varistor voltage change: Within ±10%. IEC61000-4-5 standard 10/1000us current pulse	① Temperature: 25±5℃ ② Humidity: 30% to 65% RH ③ Number of hit: 1 time ④ Pulse waveform: 10/1000 us ⑤ Applied energy: maximum surge energy (E_T) ⑥ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
16. ESD Life	① No visible mechanical damage. ② Varistor voltage change: Within ±10%. IEC61000-4-2 standard ESD gun C=150pF R=330Ω	① Discharge: Contact discharge ② Voltage: 8000V (Level 4) ③ Polarity: +, - ④ Number: 10 times within 10 sec ⑤ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
17. ESD Test	① No visible mechanical damage. ② Varistor voltage change: Within ±10%. IEC61000-4-2 standard ESD gun C=150pF R=330Ω	① Discharge: Air discharge ② Voltage: 15000V (Special level) ③ Polarity: +, - ④ Number: 10 times within 10 sec ⑤ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.

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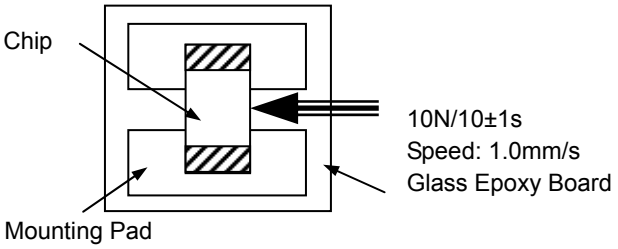
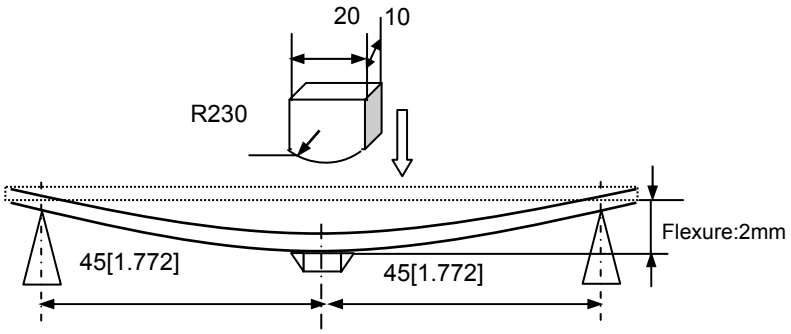
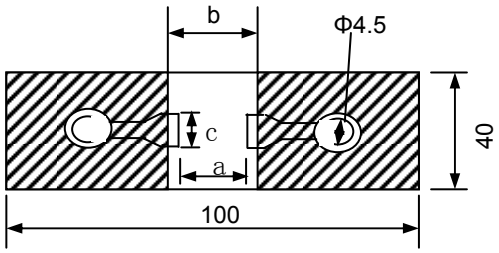
RELIABILITY AND TEST CONDITIONS

Multilayer Chip Varistor for Surge Current (SDVL Series)

<table>
<tr><th>Items</th><th>Requirements</th><th>Test Methods and Remarks</th></tr>
<tr><td>1. Operating Temperature Range</td><td colspan="2">-55℃ to +85℃</td></tr>
<tr><td>2. Storage Temperature Range</td><td colspan="2">-55℃ to +85℃</td></tr>
<tr><td>3. Terminal Strength</td><td>No removal or split of the termination or other defects shall occur.</td><td>① Solder the chip to the testing jig (glass epoxy board shown as the following figure.) using eutectic solder. Then apply a force in the direction of the arrow.
② 10N force for SDVL3216, 3225, 4532, 5650, 8063 and 10080 series.
③ Keep time: 10±1s
 
</td></tr>
<tr><td rowspan="2">4. Resistance to Flexure</td><td>No visible mechanical damage.</td><td>① Solder the chip to the test jig (glass epoxy board) using a eutectic solder. Then apply a force in the direction shown as the following figure.
② Flexure: 2mm
③ Pressurizing speed: 0.5mm/sec
④ Keep time: ≥30 sec</td></tr>
<tr><td colspan="2"> 

Unit: mm [inch]
 

Type	a	b	c
3216[1206]	2.2	5.0	2.0
3225[1210]	2.1	4.5	3.0
4532[1812]	3.0	6.0	3.8
5650[2220]	4.2	7.2	5.7
8063[3225]	4.5	6.5	3.5
10080[4032	6.5	8.5	3.5
</td></tr>
</table>

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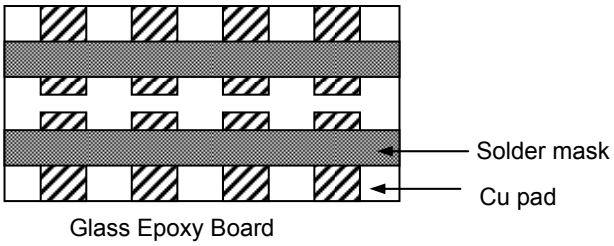
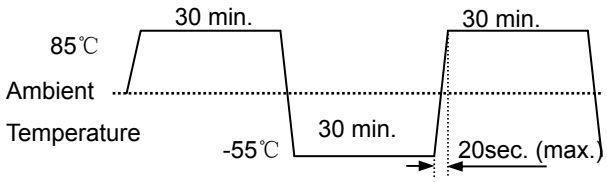
RELIABILITY AND TEST CONDITIONS

Multilayer Chip Varistor for Surge Current (SDVL Series)

Items	Requirements	Test Methods and Remarks
5. Vibration	No visible mechanical damage.	① Solder the chip to the testing jig (glass epoxy board shown as the following figure) using eutectic solder. ② The chip shall be subjected to a simple harmonic motion having total amplitude of 1.5 mm, the frequency being varied uniformly between the approximate limits of 10 and 55 Hz. ③ The frequency range from 10 to 55 Hz and return to 10 Hz shall be traversed in approximately 1 minute. This motion shall be applied for a period of 2 hours in each 3 mutually perpendicular directions (total of 6 hours). 
6. Solderability	① No visible mechanical damage. ② Wetting shall be exceeded 90% coverage.	① Solder temperature: 240±2℃ ② Duration: 3 sec ③ Solder: Sn/3.0Ag/0.5Cu ④ Flux: 25% Resin and 75% ethanol in weight
7. Resistance to Soldering Heat	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Solder temperature: 260±3℃ ② Duration: 5 sec ③ Solder: Sn/3.0Ag/0.5Cu ④ Flux: 25% Resin and 75% ethanol in weight. ⑤ The chip shall be stabilized at normal condition for 1~2 hours before measuring.
8. Thermal Shock	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature and time: -55℃ for 30±3 min→85℃ for 30±3min ② Transforming interval: Max. 20 sec ③ Tested cycle: 100 cycles ④ The chip shall be stabilized at normal condition for 1~2 hours before measuring. 
9. Resistance to Low Temperature	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: -55±2℃ ② Duration: 1000^{+24} hours ③ The chip shall be stabilized at normal condition for 1~2 hours before measuring.
10. Resistance to High Temperature	① No visible mechanical damage. ② Varistor voltage change: within ±10%.	① Temperature: 85±2℃. ② Duration: 1000^{+24} hours. ③ The chip shall be stabilized at normal condition for 1~2 hours before measuring.

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RELIABILITY AND TEST CONDITIONS

Multilayer Chip Varistor for Surge Current (SDVL Series)

Items	Requirements	Test Methods and Remarks
11. Damp Heat (Steady States)	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: 60±2℃ ② Humidity: 90% to 95% RH ③ Duration: 1000^{+24} hours ④ The chip shall be stabilized at normal condition for 1~2 hours before measuring.
12. Loading Under Damp Heat	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: 60±2℃ ② Humidity: 90% to 95% RH ③ Duration: 1000^{+24} hours ④ Applied voltage: DC working voltage ⑤ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
13. Loading at High Temperature (Life Test)	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: 85±2℃ ② Duration: 1000^{+24} hours ③ Applied voltage: DC working voltage ④ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
14. Maximum Surge Current	① No visible mechanical damage. ② Varistor voltage change: Within ±10%. IEC61000-4-5 standard 1.2/50us-8/20us voltage-current combination pulse	① Temperature: 25±5℃ ② Humidity: 30% to 65% RH ③ Number of hit: each 1 time of +/- polarity. ④ Pulse waveform: 8/20 us ⑤ Applied current: maximum surge current (I_P) ⑥ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
15. Maximum Surge Energy	① No visible mechanical damage. ② Varistor voltage change: Within ±10%. IEC61000-4-5 standard 10/1000us current pulse	① Temperature: 25±5℃ ② Humidity: 30% to 65% RH ③ Number of hit: 1 time ④ Pulse waveform: 10/1000 us ⑤ Applied energy: maximum surge energy (E_T) ⑥ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.

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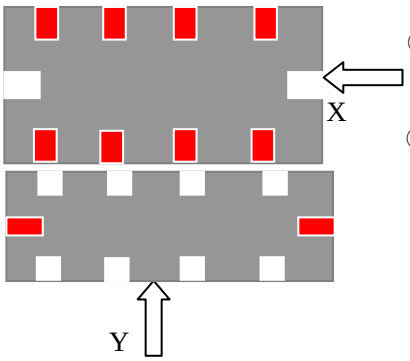
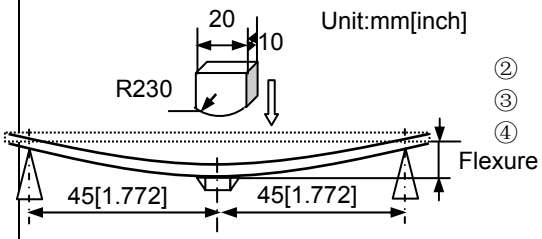
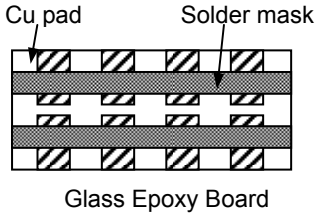
RELIABILITY AND TEST CONDITIONS

Multilayer Chip Varistor Array (SDVA-VA Series)

Items	Requirements	Test Methods and Remarks
1. Operating Temperature Range	-55℃ to +125℃	
2. Storage Temperature Range	-55℃ to +125℃	
3. Terminal Strength	No removal or split of the termination or other defects shall occur. 	① Solder the chip to the testing jig (glass epoxy board shown as the **left Fig**) using eutectic solder. Then apply a force in the direction of the arrow ② 10N force for SDV2080, SDV2082 series in X direction, 5N force for SDV2082 series in Y direction ③ Keep time: 10±1s.
4. Resistance to Flexure	No visible mechanical damage. 	① Solder the chip to the test jig (glass epoxy board shown as **the left Fig.**) using a eutectic solder. Then apply a force in the direction shown the **left Fig.** ② Flexure: 2mm. ③ Pressurizing Speed: 0.5mm/sec. ④ Keep time: 30 sec.
5. Vibration	No visible mechanical damage. 	① Solder the chip to the testing jig (glass epoxy board shown as the **left Fig.**) using eutectic solder. ② The chip shall be subjected to a simple harmonic motion having total amplitude of 1.5mm, the frequency being varied uniformly between the approximate limits of 10 and 55 Hz. ③ The frequency range from 10 to 55 Hz and return to 10 Hz shall be traversed in approximately 1 minute. This motion shall be applied for a period of 2 hours in each 3mutually perpendicular directions (total of 6 hours).
6. Solderability	① No visible mechanical damage. ② Wetting shall exceed 90% coverage.	① Solder temperature: 240±2℃ ② Duration: 3 sec. ③ Solder: Sn/3.0Ag/0.5Cu. ④ Flux: 25% Resin and 75% ethanol in weight.
7. Resistance to Soldering Heat	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Solder the chip to the testing jig ② Solder temperature: 260±3℃, re-flowing 2 times ③ Duration: 5sec. ④ The chip shall be stabilized at normal condition for 1~2 hours before measuring. ⑤ Solder: Sn/3.0Ag/0.5Cu. ⑥ Flux: 25% Resin and 75% ethanol in weight.

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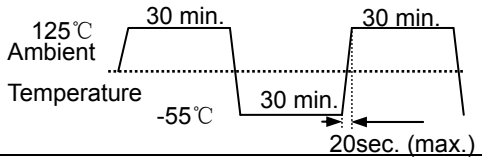
RELIABILITY AND TEST CONDITIONS

Multilayer Chip Varistor Array (SDVA-VA Series)

Items	Requirements	Test Methods and Remarks
8. Thermal Shock	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature, Time: -55℃for 30±3 min→125℃ for 30±3min. ② Transforming interval: 20sec. (max.) ③ Tested cycle: 100 cycles. ④ The chip shall be stabilized at normal condition for 1~2 hours before measuring. 
9. Resistance to Low Temperature	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: -55±2℃ ② Duration: 1000^{+24} hours. ③ The chip shall be stabilized at normal condition for 1~2 hours before measuring.
10. Loading Under Damp Heat	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: 60±2℃ ② Humidity: 90% to 95% RH. ③ Duration: 1000^{+24} hours. ④ Applied voltage: DC Working Voltage. ⑤ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
11. Loading at High Temperature (Life Test)	① No visible mechanical damage. ② Varistor voltage change: Within ±10%.	① Temperature: 125±2℃ ② Duration: 1000^{+24} hours. ③ Applied voltage: DC Working Voltage. ④ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
12. Maximum Surge Current	① No visible mechanical damage. ② Varistor voltage change: Within ±10%. IEC61000-4-5 standard 1.2/50us-8/20us voltage-current combination pulse	① Temperature: 25±5℃ ② Humidity: 30% to 65% RH. ③ Number of hit: each 1 time of +/- polarity. ④ Pulse waveform: 8/20 us. ⑤ Applied current: maximum surge current (I_P). ⑥ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
13. ESD Life	① No visible mechanical damage. ② Varistor voltage change: Within ±10%. IEC61000-4-2 standard ESD gun C=150pF R=330Ω	① Discharge: Contact discharge. ② Voltage: 8000V (Level 4). ③ Polarity: +, -. ④ Number: 10 times within 10 sec. ⑤ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
14. ESD Test	① No visible mechanical damage. ② Varistor voltage change: Within ±10%. IEC61000-4-2 standard ESD gun C=150pF R=330Ω	① Discharge: Air discharge. ② Voltage: 15000V (Special level). ③ Polarity: +, - ④ Number: 10 times within 10 sec. ⑤ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.

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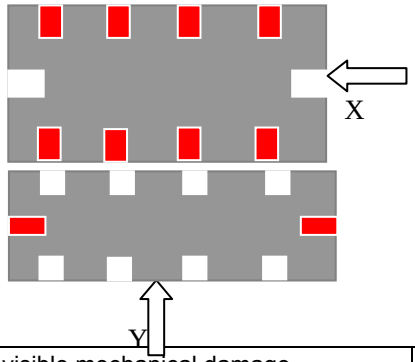
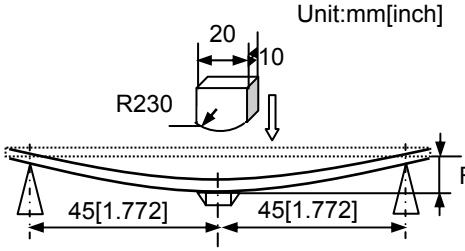
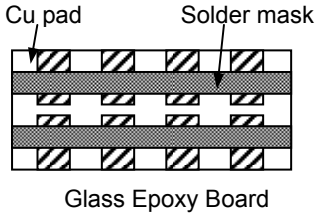
RELIABILITY AND TEST CONDITIONS

Multilayer Chip Varistor Array (SDVA-R Series)

Items	Requirements	Test Methods and Remarks
1. Operating Temperature Range	-55℃ to +125℃	
2. Storage Temperature Range	-55℃ to +125℃	
3. Terminal Strength	No removal or split of the termination or other defects shall occur. 	④ Solder the chip to the testing jig (glass epoxy board shown as the **left Fig**) using eutectic solder. Then apply a force in the direction of the arrow ⑤ 10N force in X direction and 5N in Y direction ⑥ Keep time: 10±1s.
4. Resistance to Flexure	No visible mechanical damage. 	⑤ Solder the chip to the test jig (glass epoxy board shown as **the left Fig.**) using a eutectic solder. Then apply a force in the direction shown the **left Fig.** ⑥ Flexure: 2mm. ⑦ Pressurizing Speed: 0.5mm/sec. ⑧ Keep time: 30 sec.
5. Vibration	No visible mechanical damage. 	⑤ Solder the chip to the testing jig (glass epoxy board shown as the **left Fig.**) using eutectic solder. ⑥ The chip shall be subjected to a simple harmonic motion having total amplitude of 1.5mm, the frequency being varied uniformly between the approximate limits of 10 and 55 Hz. ⑦ The frequency range from 10 to 55 Hz and return to 10 Hz shall be traversed in approximately 1 minute. This motion shall be applied for a period of 2 hours in each 3mutually perpendicular directions (total of 6 hours).
6. Solderability	③ No visible mechanical damage. ④ Wetting shall exceed 90% coverage.	⑦ Solder temperature: 240±2℃ ⑧ Duration: 3 sec. ⑨ Solder: Sn/3.0Ag/0.5Cu. ⑧ Flux: 25% Resin and 75% ethanol in weight.
7. Resistance to Soldering Heat	③ No visible mechanical damage. ④ Varistor voltage change: Within ±10%.	④ Solder the chip to the testing jig ⑤ Solder temperature: 260±3℃, re-flowing 2 times ⑥ Duration: 5sec. ⑩ The chip shall be stabilized at normal condition for 1~2 hours before measuring. ⑪ Solder: Sn/3.0Ag/0.5Cu. ⑫ Flux: 25% Resin and 75% ethanol in weight.

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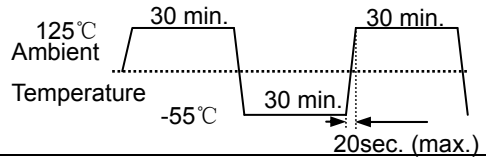
RELIABILITY AND TEST CONDITIONS

Multilayer Chip Varistor Array (SDVA-R Series)

Items	Requirements	Test Methods and Remarks
8. Thermal Shock	③ No visible mechanical damage. ④ Varistor voltage change: Within ±10%.	⑤ Temperature, Time: -55℃for 30±3 min→125℃ for 30±3min. ⑥ Transforming interval: 20sec. (max.) ⑦ Tested cycle: 100 cycles. ⑧ The chip shall be stabilized at normal condition for 1~2 hours before measuring. 
9. Resistance to Low Temperature	③ No visible mechanical damage. ④ Varistor voltage change: Within ±10%.	④ Temperature: -55±2℃ ⑤ Duration: 1000^{+24} hours. ⑥ The chip shall be stabilized at normal condition for 1~2 hours before measuring.
10. Loading Under Damp Heat	③ No visible mechanical damage. ④ Varistor voltage change: Within ±10%.	⑥ Temperature: 60±2℃ ⑦ Humidity: 90% to 95% RH. ⑧ Duration: 1000^{+24} hours. ⑨ Applied voltage: DC Working Voltage. ⑩ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
11. Loading at High Temperature (Life Test)	③ No visible mechanical damage. ④ Varistor voltage change: Within ±10%.	⑤ Temperature: 125±2℃ ⑥ Duration: 1000^{+24} hours. ⑦ Applied voltage: DC Working Voltage. ⑧ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
12. Maximum Surge Current	③ No visible mechanical damage. ④ Varistor voltage change: Within ±10%. IEC61000-4-5 standard 1.2/50us-8/20us voltage-current combination pulse	⑦ Temperature: 25±5℃ ⑧ Humidity: 30% to 65% RH. ⑨ Number of hit: each 1 time of +/- polarity. ⑩ Pulse waveform: 8/20 us. ⑪ Applied current: maximum surge current (I_P). ⑫ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
13. ESD Life	③ No visible mechanical damage. ④ Varistor voltage change: Within ±10%. IEC61000-4-2 standard ESD gun C=150pF R=330Ω	⑥ Discharge: Contact discharge. ⑦ Voltage: 8000V (Level 4). ⑧ Polarity: +, -. ⑨ Number: 10 times within 10 sec. ⑩ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.
14. ESD Test	③ No visible mechanical damage. ④ Varistor voltage change: Within ±10%. IEC61000-4-2 standard ESD gun C=150pF R=330Ω	⑥ Discharge: Air discharge. ⑦ Voltage: 15000V (Special level). ⑧ Polarity: +, - ⑨ Number: 10 times within 10 sec. ⑩ The chip shall be stabilized at normal condition for 1~2 hours before positive and negative direction measuring.

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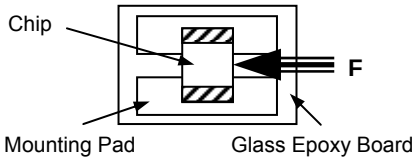
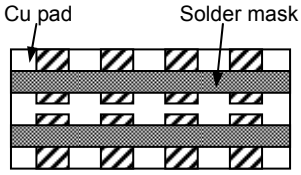
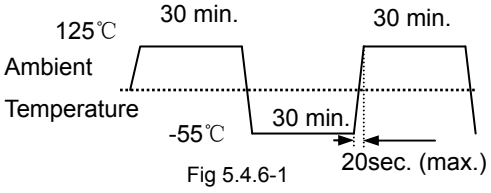
RELIABILITY AND TEST CONDITIONS

Glass Ceramic ESD Suppressor (GESD Series)

Items	Requirements	Test Methods and Remarks
5.4.1. Terminal Strength	No removal or split of the termination or other defects shall occur.  **Fig.5.4.1-1**	① Solder the chip to the testing jig (glass epoxy board shown in **Fig.5.4.1-1**) using eutectic solder. Then apply a force in the direction of the arrow. ② 2N force for GESD0603 series, ③ 5N force for GESD1005 and 1608 series ④ Keep time: 10±1s.
5.4.3 Vibration	No visible mechanical damage.  **Fig. 5.4.3-1**	① Solder the chip to the testing jig (glass epoxy board shown in **Fig.5.4.3-1**) using eutectic solder. ② The chip shall be subjected to a simple harmonic motion having total amplitude of 1.5mm, the frequency being varied uniformly between the approximate limits of 10 and 55 Hz. ③ The frequency range from 10 to 55 Hz and return to 10 Hz shall be traversed in approximately 1 minute. This motion shall be applied for a period of 2 hours in each 3mutually perpendicular directions (total of 6 hours).
5.4.4 Solderability	① No visible mechanical damage. ② Leakage Current @ V_{DC} change: within 1μA	① Solder temperature: 240±2℃ ② Duration: 3 sec. ③ Solder: Sn/3.0Ag/0.5Cu. ④ Flux: 25% Resin and 75% ethanol in weight. ⑤ The chip shall be stabilized at normal condition for 24±4 hours before measuring.
5.4.5 Resistance to Soldering Heat	① No visible mechanical damage. ② Leakage Current @ V_{DC} change: within 1μA	① Solder temperature: 260±3℃ ② Duration: 5 sec. ③ The chip shall be stabilized at normal condition for 24±4 hours before measuring. ④ Solder: Sn/3.0Ag/0.5Cu. ⑤ Flux: 25% Resin and 75% ethanol in weight.
5.4.6 Thermal Shock	① No visible mechanical damage. ② Leakage Current @ V_{DC} change: within 1μA  Fig 5.4.6-1	① Temperature, Time: -55℃for 30±3 min→125℃ for 30±3min. ② Transforming interval: 20sec. (max.) ③ Tested cycle: 100 cycles. ④ The chip shall be stabilized at normal condition for 24±4 hours before measuring.
5.4.7 Resistance to Low Temperature	① No visible mechanical damage. ② Leakage Current @ V_{DC} change: within 1μA	① Temperature: -55±2℃ ② Duration: 1000^{+24} hours. ③ The chip shall be stabilized at normal condition for 24±4 hours before measuring.
5.4.8 Resistance to High Temperature	① No visible mechanical damage. ② Leakage Current @ V_{DC} change: within 1μA	① Temperature: 125±2℃. ② Duration: 1000^{+24} hours. ③ The chip shall be stabilized at normal condition for 24±4 hours before measuring.

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RELIABILITY AND TEST CONDITIONS

Glass Ceramic ESD Suppressor (GESD Series)

Items	Requirements	Test Methods and Remarks
5.4.9 Damp Heat (Steady States)	① No visible mechanical damage. ② Leakage Current @ V_{DC} change: Within 1μA	① Temperature: 60±2℃ ② Humidity: 90% to 95% RH. ③ Duration: 1000^{+24} hours. ④ The chip shall be stabilized at normal condition for 24±4 hours before measuring.
5.4.10 Loading Under Damp Heat	① No visible mechanical damage. ② Leakage Current @ V_{DC} change: within 1μA	① Temperature: 60±2℃ ② Humidity: 90% to 95% RH. ③ Duration:1000^{+24} hours. ④ Applied voltage: DC Working Voltage. ⑤ The chip shall be stabilized at normal condition for 24±4 hours before measuring.
5.4.11 Loading at High Temperature (Life Test)	① No visible mechanical damage. ② Leakage Current @ V_{DC} change: within 1μA	① Temperature: 125±2℃ ② Duration:1000^{+24} hours. ③ Applied voltage: DC Working Voltage. ④ The chip shall be stabilized at normal condition for 24±4 hours before measuring.
5.4.12 ESD Life	① No visible mechanical damage. ② Leakage Current @ V_{DC} change: within 100nA IEC61000-4-2 standard ESD gun C=150pF R=330Ω	① Discharge: Contact discharge. ② Voltage: 8000V (Level 4). ③ Polarity: +, -. ④ Number: 10 times within 10 sec. ⑤ The chip shall be stabilized at normal condition for 1~2 hours before measuring.

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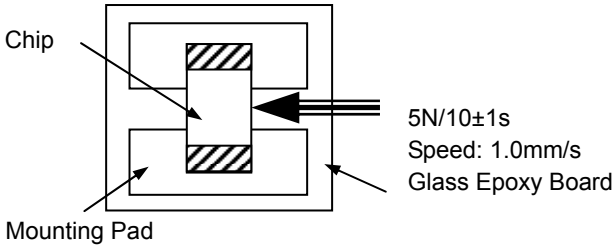
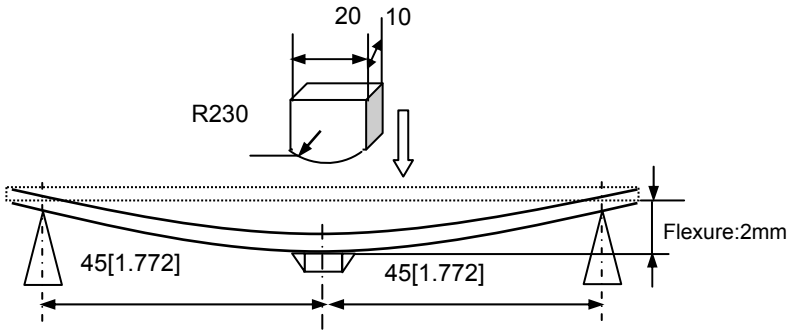
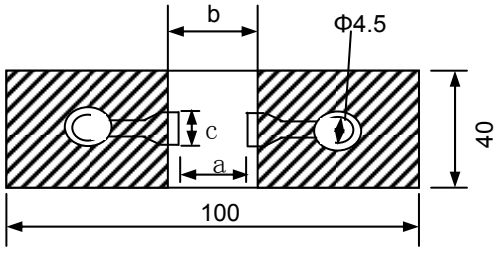
RELIABILITY AND TEST CONDITIONS

Chip Polymer ESD Suppressor (PESD Series)

<table>
<tr><th>Items</th><th>Requirements</th><th>Test Methods and Remarks</th></tr>
<tr><td>1. Operating Temperature Range</td><td colspan="2">-40℃ to +85℃</td></tr>
<tr><td>2. Storage Temperature Range</td><td colspan="2">-40℃ to +85℃</td></tr>
<tr><td>3. Terminal Strength</td><td>No removal or split of the termination or other defects shall occur.</td><td>① Solder the chip to the testing jig (glass epoxy board shown as the following figure.) using eutectic solder. Then apply a force in the direction of the arrow.
② 5N force for PESD1005 and 1608 series.
③ Keep time: 10±1s
 
</td></tr>
<tr><td rowspan="2">4. Resistance to Flexure</td><td>No visible mechanical damage.</td><td>① Solder the chip to the test jig (glass epoxy board) using a eutectic solder. Then apply a force in the direction shown as the following figure.
② Flexure: 2mm
③ Pressurizing speed: 0.5mm/sec
④ Keep time: 30sec</td></tr>
<tr><td colspan="2"> 

Unit: mm [inch]
 

Type	a	b	c
1005[0402]	0.4	1.5	0.5
1608[0603]	1.0	3.0	1.2
</td></tr>
</table>

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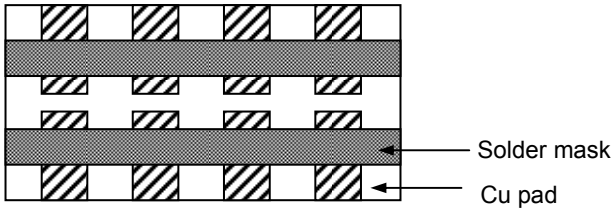
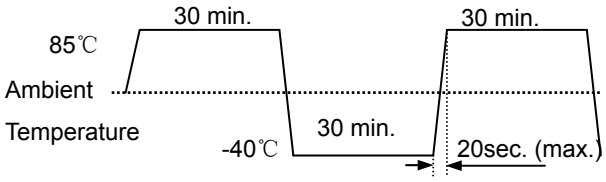
RELIABILITY AND TEST CONDITIONS

Chip Polymer ESD Suppressor (PESD Series)

Items	Requirements	Test Methods and Remarks
5. Vibration	No visible mechanical damage.	① Solder the chip to the testing jig (glass epoxy board shown as the following figure) using eutectic solder. ② The chip shall be subjected to a simple harmonic motion having total amplitude of 1.5 mm, the frequency being varied uniformly between the approximate limits of 10 and 55 Hz. ③ The frequency range from 10 to 55 Hz and return to 10 Hz shall be traversed in approximately 1 minute. This motion shall be applied for a period of 2 hours in each 3 mutually perpendicular directions (total of 6 hours).  Glass Epoxy Board
6. Solderability	① No visible mechanical damage. ② Leakage Current @V_{DC} change: within 10μA.	① Solder temperature: 240±2℃ ② Duration: 3 sec ③ Solder: Sn/3.0Ag/0.5Cu ④ Flux: 25% Resin and 75% ethanol in weight ⑤ The chip shall be stabilized at normal condition for 24±4 hours before measuring.
7. Resistance to Soldering Heat	① No visible mechanical damage. ② Leakage Current @V_{DC} change: within 10μA.	① Solder temperature: 260±3℃ ② Duration: 5 sec ③ Solder: Sn/3.0Ag/0.5Cu ④ Flux: 25% Resin and 75% ethanol in weight. ⑤ The chip shall be stabilized at normal condition for 24±4 hours before measuring.
8. Thermal Shock	① No visible mechanical damage. ② Leakage Current @V_{DC} change: within 10 μ A.	① Temperature and time: -40℃ for 30±3 min→85℃ for 30±3min ② Transforming interval: Max. 20 sec ③ Tested cycle: 100 cycles ④ The chip shall be stabilized at normal condition for 24±4 hours before measuring. 
9. Resistance to Low Temperature	① No visible mechanical damage. ② Leakage Current @V_{DC} change: within 10 μ A.	① Temperature: -40±2℃ ② Duration: 1000^{+24} hours ③ The chip shall be stabilized at normal condition for 24±4 hours before measuring.
10. Resistance to High Temperature	① No visible mechanical damage. ② Leakage Current @V_{DC} change: within 10 μ A.	① Temperature: 85±2℃. ② Duration: 1000^{+24} hours. ③ The chip shall be stabilized at normal condition for 24±4 hours before measuring.

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RELIABILITY AND TEST CONDITIONS

Chip Polymer ESD Suppressor (PESD Series)

Items	Requirements	Test Methods and Remarks
11. Damp Heat (Steady States)	① No visible mechanical damage. ② Leakage Current @V_{DC} change: within 10 μA..	① Temperature: 55±2℃ ② Humidity: 90% to 95% RH ③ Duration: 1000^{+24} hours ④ The chip shall be stabilized at normal condition for 24±4 hours before measuring.
12. Loading Under Damp Heat	① No visible mechanical damage. ② Leakage Current @V_{DC} change: within 10 μA.	① Temperature: 55±2℃ ② Humidity: 90% to 95% RH ③ Duration: 500^{+24} hours ④ Applied voltage: DC working voltage ⑤ The chip shall be stabilized at normal condition for 24±4 hours measuring.
13. Loading at High Temperature (Life Test)	① No visible mechanical damage. ② Leakage Current @V_{DC} change: within 10 μA..	① Temperature: 85±2℃ ② Duration: 500^{+24} hours ③ Applied voltage: DC working voltage ④ The chip shall be stabilized at normal condition for 24±4 hours before measuring.
14. ESD Life	① No visible mechanical damage. ② Leakage Current @V_{DC} change: within 10 μA IEC61000-4-2 standard ESD gun C=150pF R=330Ω	① Discharge: Contact discharge. ② Voltage: 8000V (Level 4). ③ Polarity: +, -. ④ Number: 10 times within 10 sec. ⑤ The chip shall be stabilized at normal condition for 1~2 hours before measuring.

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RELIABILITY AND TEST CONDITIONS

Leaded Varistor for Voltage Surge Suppresssion VPR Series)

<table>
<tr><th>Items</th><th>Requirements</th><th>Test Methods</th></tr>
<tr><td>1. Operating Temperature Range</td><td colspan="2">-40℃ to +85℃</td></tr>
<tr><td>2. Storage Temperature Range</td><td colspan="2">-40℃ to +85℃</td></tr>
<tr><td>3. Robustness of Terminations (Tensile)</td><td rowspan="3">No outstanding damage</td><td>After gradually applying the force specified below and keeping the unit fixed for the seconds,the terminal shall be visually examined for any damage.
<table><tr><th>Terminal diameter</th><th>Force</th></tr><tr><td>Ø 0.6 mm</td><td>9.8 N（1.0Kgf）</td></tr><tr><td>Ø 0.8 mm</td><td>9.8 N（1.0Kgf）</td></tr><tr><td>Ø 1.0 mm</td><td>19.6 N（2.0Kgf）</td></tr></table></td></tr>
<tr><td>4. Robustness of Terminations (Bending)</td><td>The unit shall be secured with its terminal kept vertical and the force specified below be appliedin the axial direction.
The terminal shall gradually be bent by 90° in one direction, then 90°in the opposite direction,and again back to the original position.
<table><tr><th>Terminal diameter</th><th>Force</th></tr><tr><td>Ø 0.6 mm</td><td>4.9 N（0.5Kgf）</td></tr><tr><td>Ø 0.8 mm</td><td>4.9 N（0.5Kgf）</td></tr><tr><td>Ø 1.0 mm</td><td>9.8 N（1.0Kgf）</td></tr></table></td></tr>
<tr><td>5. Vibration</td><td>After repeat applying a single harmonic vibration (amplitude: 0.75 mm) double amplitude:1.5mm with 1 minute vibration frequency cycles (10Hz to 55Hz to10Hz) to each of three perpendicular directions for 2 hours. Thereafter, the unit shall be visually examined.</td></tr>
<tr><td>6. Solderability</td><td>Approximately 95% of the terminals shall be covered with solder uniformly</td><td>After dipping the terminals to a depth of approximately 3mm from the body in a soldering bath of 235±5℃ for 2±0.5 seconds, the terminal shall be visually examined.</td></tr>
<tr><td>7. Resistance to Soldering Heat</td><td>△Vb/Vb≦±5%
No outstanding damage</td><td>After each lead shall be dipped into a solder bath having a temperature 260±5℃,to a point 2.0 to 2.5 mm from the body of the unit, using shielding board (t=1.5mm), be held there for specified time (5 series: 5±1s and others: 10±1s), and then be stored at room temperature and humidity for 1 to 2 hours. The change of VcmA and mechanical damages are examined.</td></tr>
<tr><td>8. Temperature Coefficient of Varistor Voltage</td><td>－0.05 %/℃ max</td><td>$\frac{\text{Vb at 85℃} - \text{Vb at 25℃}}{\text{Vb at 25℃}} \times 1/60 \times 100(\%/℃)$</td></tr>
<tr><td>9.Capacitance</td><td>To meet the specified value</td><td>Capacitance shall be measured at 1 kHZ ±10 %, 1Vrms max. 0V bias and 20±2℃</td></tr>
<tr><td>10. Withstanding Voltage (Body Insulation)</td><td>No breakdown</td><td>The specified voltage shall be applied both terminals of the specimen connected together and metal foil closely wrapped round its body for 1 minute. Electrical breakdown shall be examined.
<table><tr><th>Classification
(Nominal varistor voltage)</th><th>Test Voltage
(AC)</th></tr><tr><td>V ACrms ≦210V</td><td>1000 Vrms</td></tr><tr><td>V ACrms ＞210V</td><td>1500 Vrms</td></tr></table></td></tr>
</table>

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RELIABILITY AND TEST CONDITIONS

Leaded Varistor for Voltage Surge Suppresssion VPR Series)

<table>
<tr><th>Items</th><th>Requirements</th><th>Test Methods</th></tr>
<tr><td>11.
Impulse Life
（I）</td><td rowspan="2">△V_b / V_b≦±10%</td><td>The change of Vb shall be measured after the impulse listed below is applied 10000 times continuously with the interval of ten seconds at room temperature.
<table>
<tr><td>5 Series</td><td>VPR05KD130 to VPR05KD460</td><td>20A (8/20μs)</td></tr>
<tr><td>7 Series</td><td>VPR07KD130 to VPR07KD510</td><td>50A (8/20μs)</td></tr>
<tr><td>10 Series</td><td>VPR10KD130 to VPR10KD680</td><td>100A (8/20μs)</td></tr>
<tr><td>14 Series</td><td>VPR14KD130 to VPR14KD680</td><td>150A (8/20μs)</td></tr>
<tr><td>20 Series</td><td>VPR20KD130 to VPR20KD680</td><td>200A (8/20μs)</td></tr>
</table></td></tr>
<tr><td>12.
Impulse Life
（II）</td><td>The change of Vb shall be measured after the impulse listed below is applied 100000 times continuously with the interval of ten seconds at room temperature.
<table>
<tr><td>5 Series</td><td>VPR05KD130 to VPR05KD460</td><td>14A (8/20μs)</td></tr>
<tr><td>7 Series</td><td>VPR07KD130 to VPR07KD510</td><td>35A (8/20μs)</td></tr>
<tr><td>10 Series</td><td>VPR10KD130 to VPR10KD680</td><td>70A (8/20μs)</td></tr>
<tr><td>14 Series</td><td>VPR14KD130 to VPR14KD680</td><td>90A (8/20μs)</td></tr>
</table></td></tr>
<tr><td>13.High Temperature Storage/Dry Heat</td><td rowspan="3">△Vb/Vb≦±5%</td><td>The specimen shall be subjected to 125±2℃ for 1000 hours in a thermostatic bath without load and then stored at room temperature and humidity for 1 to 2 hours. Thereafter, the change of Vb shall be measured.</td></tr>
<tr><td>14.amp Heat/ Humidity (Steady State)</td><td>The specimen shall be subjected to 40±2℃, 90 to 95 %RH for 1000 hours without load and then stored at room temperature and humidity for one to two hours. Thereafter, the change of Vb shall be measured.</td></tr>
<tr><td>15.
Temperature Cycle</td><td>The temperature cycle shown below shall be repeated five times and then stored at room temperature and humidity for one to two hours. The change of Vb and mechanical damage shall be examined.
<table>
<tr><th>Step</th><th>Temperature(℃)</th><th>Period (minutes)</th></tr>
<tr><td>1</td><td>-40±3</td><td>30±3</td></tr>
<tr><td>2</td><td>Room temperature</td><td>15±3</td></tr>
<tr><td>3</td><td>85±3</td><td>30±3</td></tr>
<tr><td>4</td><td>Room temperature</td><td>15±3</td></tr>
</table></td></tr>
<tr><td>16.High Temperature Load/ Dry Heat Load</td><td>△Vb/Vb≦±10%</td><td>After being continuously applied the Maximum Allowable Voltage at 85±2℃ for 1000 hours. The specimen shall be stored at room temperature and humidity for one to two hours Thereafter, the change of Vb shall be measured.</td></tr>
<tr><td>17.Damp Heat Load/ Humidity Load</td><td>△Vb/Vb≦±10%</td><td>The specimen shall be subjected to 40±2℃, 90 to 95 %RH and the Maximum Allowable Voltage for 1000 hours and then stored at room temperature and humidity for one to two hours. Thereafter, the change of Vb shall be measured.</td></tr>
<tr><td>18.Low Temperature Storage/Cold</td><td>△Vb/Vb≦±5%</td><td>The specimen shall be subjected to -40±2℃ without load for 1000 hours and then stored at room temperature for one to two hours. Thereafter, the change of Vb shall be measured.</td></tr>
</table>

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